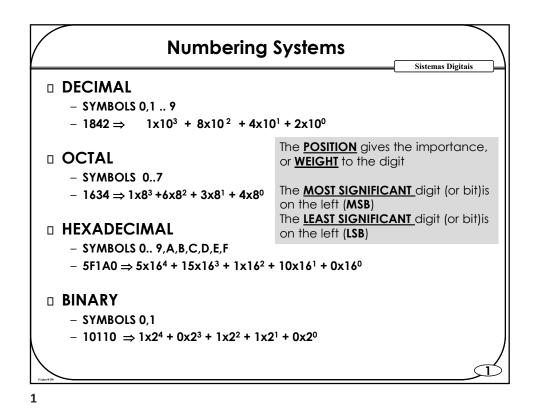
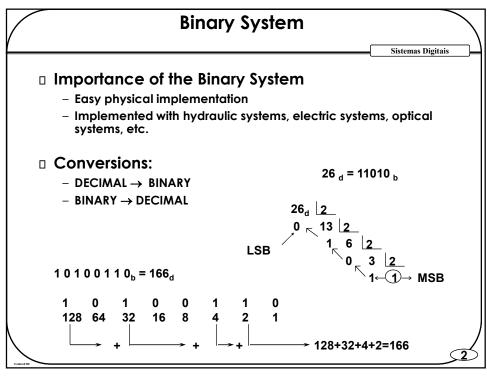
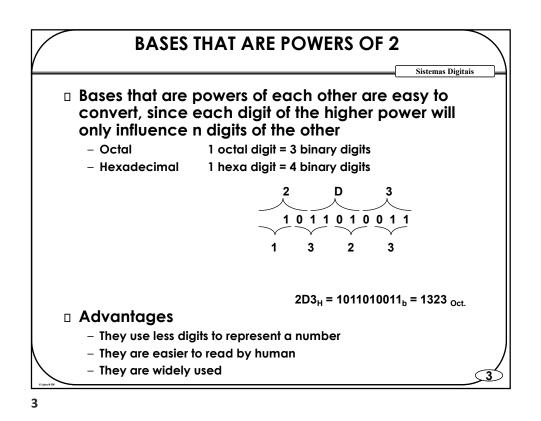
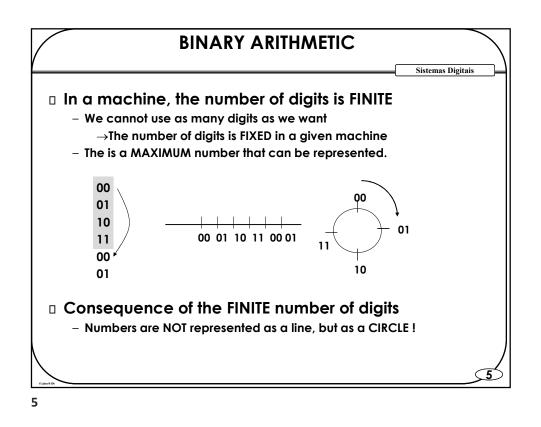
Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021

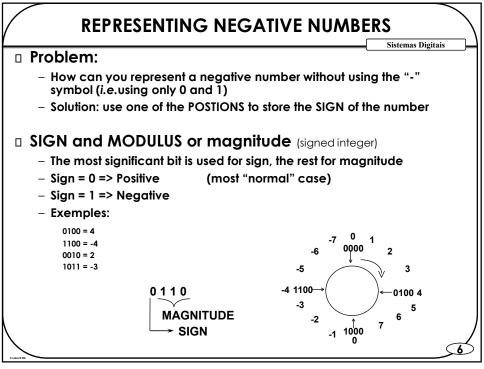




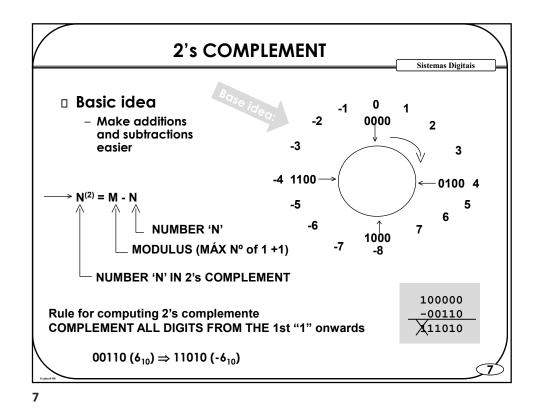


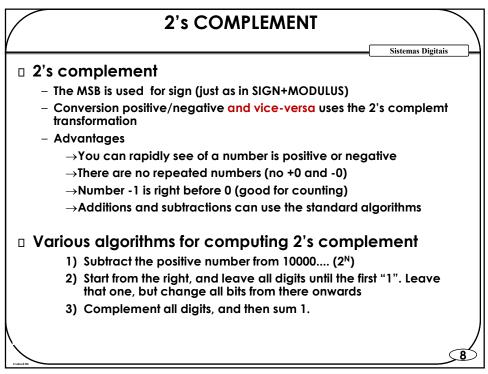
BINAR	RY ARITHMETIC	
		Sistemas Digitais
 Basically the same as Numbers are summed dig From one digit to the next 1 plus 1 is two (i.e. 10_b) Example: 	gibit by digit	
Adition ———	(11011) ₂ + (10011) ₂ (101110) ₂	(647) ₁₀ + (537) ₁₀ (1184) ₁₀
Multiplication → Only SHIFT, and COPY with a final sum !!!	1101 × 101 1101 0000 <u>1101</u> 1000001	152 × 231 152 456 <u>304</u> 35012



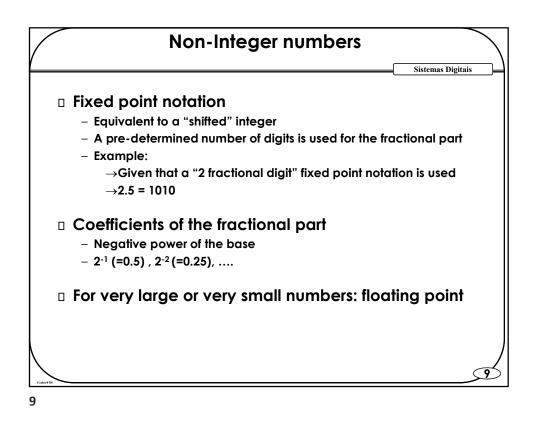


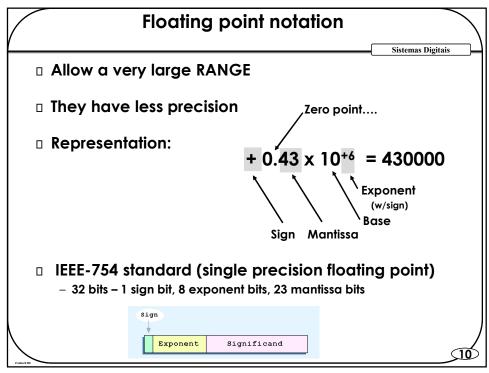
Systems, Data Representation, Boolean Algebra, Bas V.2.4 V.Lobo 2021

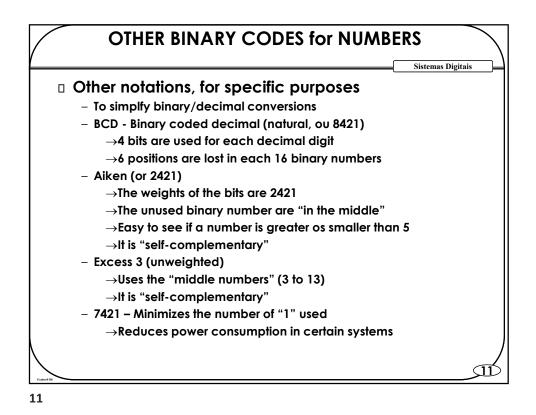




Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021

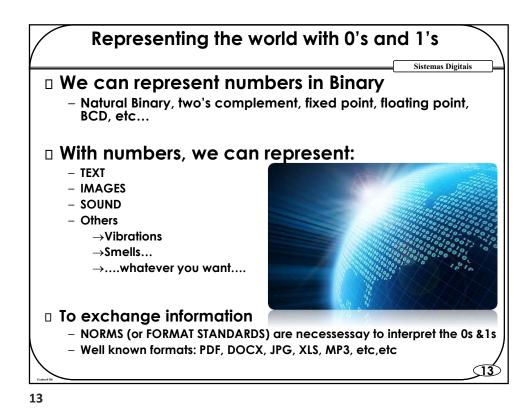


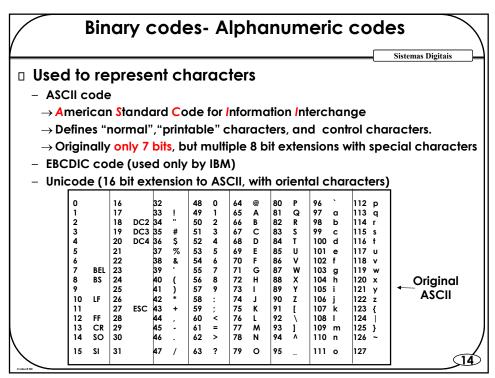




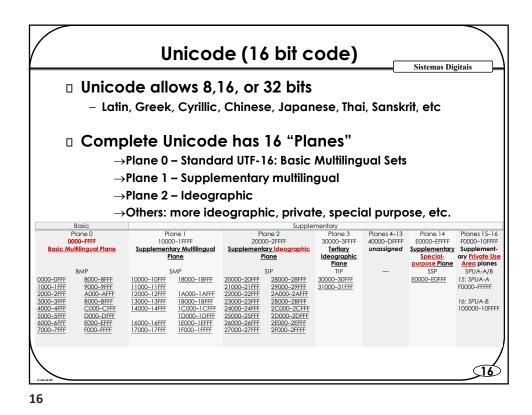
					Sistemas Digita
Dec.	BCD	AIKEN	EXC.3	7421	Gray
0	0000	0000	0011	0000	0000
1	0001	0001	0100	0001	0000
2	0010	0010	0101	0010	0001
3	0011	0011	0110	0011	0011
4	0100	0100	0111	0100	0010
5	0101	1011	1000	0101	
6	0110	1100	1001	0110	0110
7	0111	1101	1010	1000	0111
8	1000	1110	1011	1001	0101
9	1001	1111	1100	1010	
Grav	code	(reflec	ted bi	nary code)	
		•		bit changes at e	each time)
			• •	due to transitio	-
		-	• •		113
-	→Physica	al conver	ters (sen	isors)	
		c code			

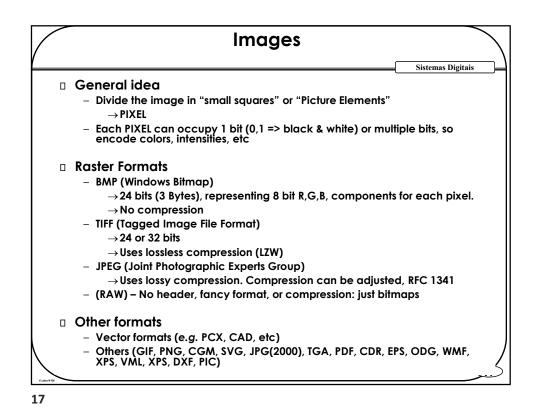
Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021

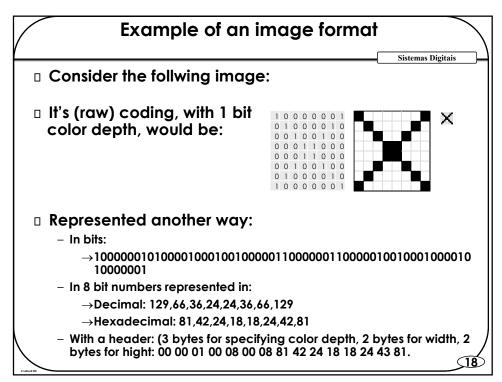


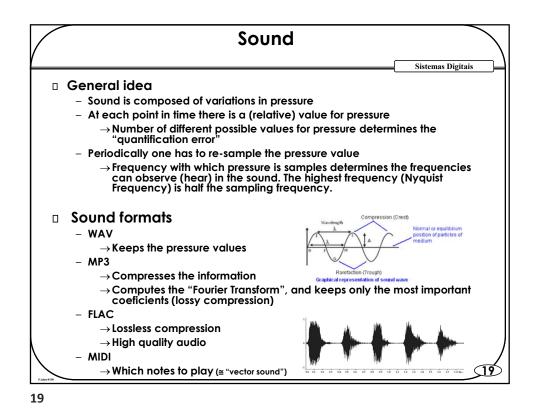


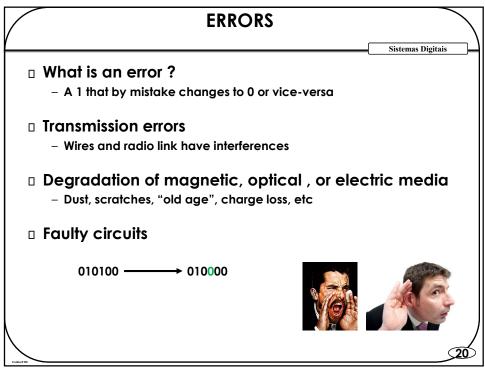
														Sist	emas	Digita
Co	de	page 8	50	(int	err	nat	ion	al.	ISO	/IE	C 8	85	9-1	. U	TF-	8)
		ili control	1	•		printa								_		- /
		aracters		A		acters			Extended ASCII characters							
	NULL	(Null character)	32	space	64	@	96		128	ç	160	á	192	L	224	Ó
01	SOH	(Start of Header)	33	1	65	A	97	а	129	ü	161	í	193	T	225	ß
02	STX	(Start of Text)	34		66	В	98	b	130	é	162	Ó	194	Т	226	Ô
03	ETX	(End of Text)	35	#	67	С	99	С	131	â	163	ú	195	-	227	Ò
04	EOT	(End of Trans.)	36	S	68	D	100	d	132	ä	164	ñ	196	-	228	õ
05	ENQ	(Enquiry)	37	%	69	E	101	e	133	à	165	Ň	197	+	229	Õ
06	ACK	(Acknowledgement)	38	8	70	F	102	f	134	å	166	a 0	198	ã	230	μ
07	BEL	(Bell)	39		71	G	103	g	135	ç	167		199	Ã	231	þ
08	BS	(Backspace)	40	(72	н	104	h	136	ê	168	5	200	L	232	P
09	HT	(Horizontal Tab)	41)	73	1	105	1	137	ë	169	•	201	1	233	Ú
10	LF	(Line feed)	42	*	74	J	106	1	138	è	170	7	202	표	234	Û
11	VT	(Vertical Tab)	43	+	75	ĸ	107	k	139	ï	171	1/2	203	T	235	Ù
12	FF	(Form feed)	44	,	76	L	108	1	140	Î	172	1/4	204	-	236	ý Ý
13	CR	(Carriage return)	45		77	м	109	m	141	ì	173	i	205	=	237	Y
14	SO	(Shift Out)	46		78	N	110	n	142	Ä	174	44	206	#	238	
15	SI	(Shift In)	47	1	79	0	111	0	143	Å	175	>>	207	-	239	
16	DLE	(Data link escape)	48	0	80	Р	112	р	144	É	176	-	208	ð	240	=
17	DC1	(Device control 1)	49	1	81	Q	113	q	145	æ	177		209	Đ	241	±
18	DC2	(Device control 2)	50	2	82	R	114	r	146	Æ	178		210	Ê	242	7.
19	DC3	(Device control 3)	51	3	83	S	115	S	147	Ô	179		211	Ë	243	
20	DC4	(Device control 4)	52	4	84	Т	116	t	148	ö	180	-	212	È	244	1
21	NAK	(Negative acknowl.)	53	5	85	U	117	u	149	ò	181	A	213	1	245	ş
22	SYN	(Synchronous idle)	54	6	86	v	118	v	150	û	182	Â	214	1	246	÷
23	ETB	(End of trans. block)	55	7	87	W	119	W	151	ù	183	Á	215	1	247	3
24	CAN	(Cancel)	56	8	88	X	120	x	152	ÿ	184	0	216	1	248	•
25	EM	(End of medium)	57	9	89	Y	121	У	153	Ö	185	1	217	1	249	
26	SUB	(Substitute)	58	:	90	Z	122	z	154	Ü	186		218	Г	250	
27	ESC	(Escape)	59	;	91	1	123	{	155	ø	187	٦	219		251	1
28	FS	(File separator)	60	<	92	1	124		156	£	188	크	220		252	3
29	GS	(Group separator)	61	=	93	1	125	}	157	ø	189	¢	221	1	253	
30	RS	(Record separator)	62	>	94	^	126	~	158	×	190	¥	222	1	254	
31	US	(Unit separator)	63	?	95	- 23			159	f	191	٦	223	1	255	nbsp
127	DEL	(Delete)														

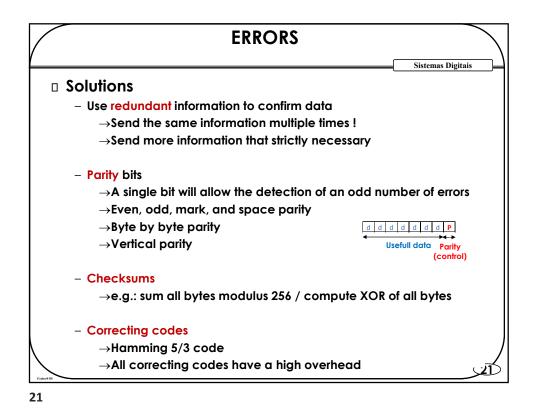


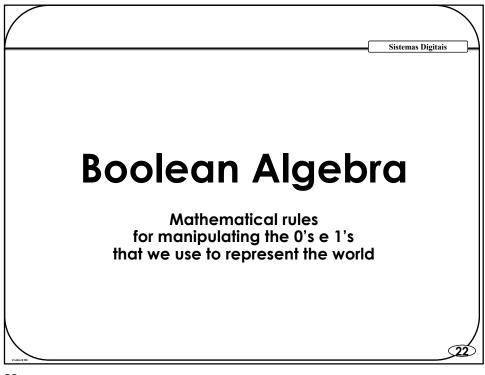




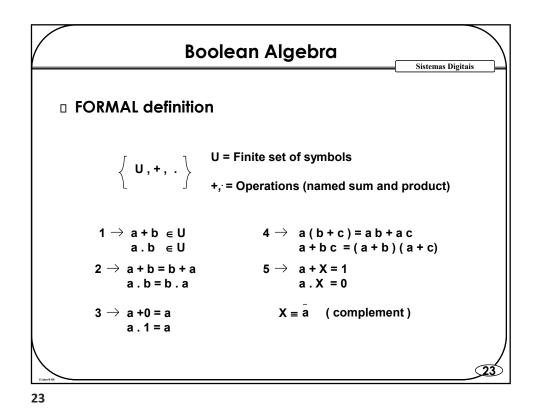


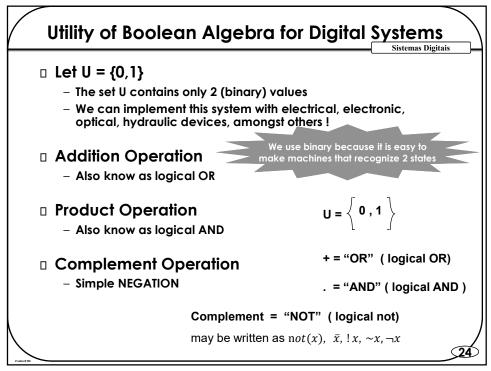




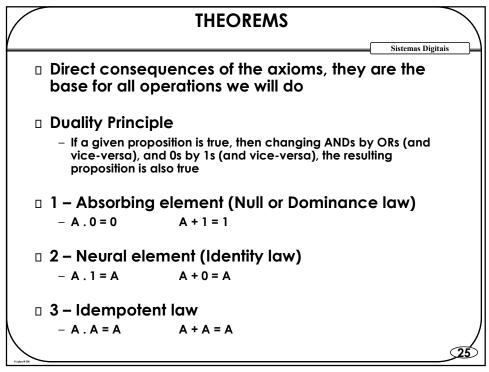


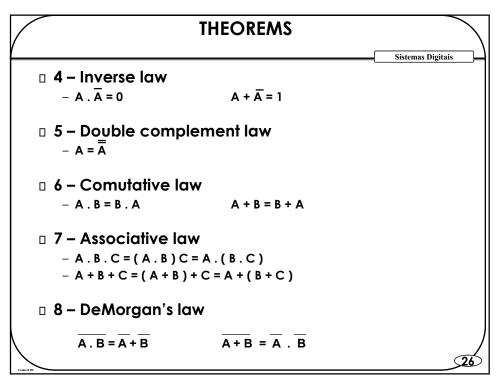
Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021



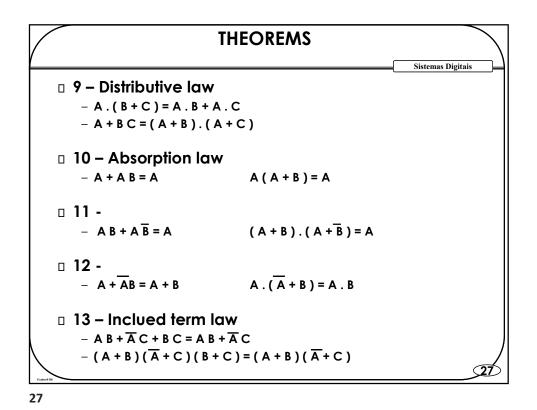


Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021





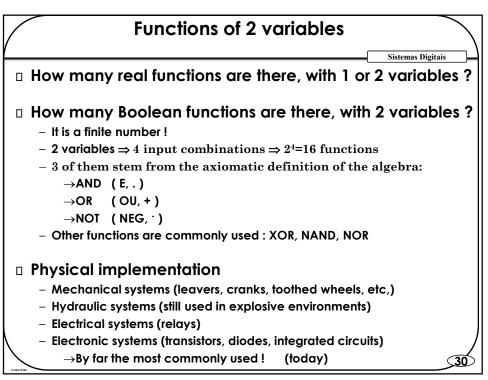
Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021



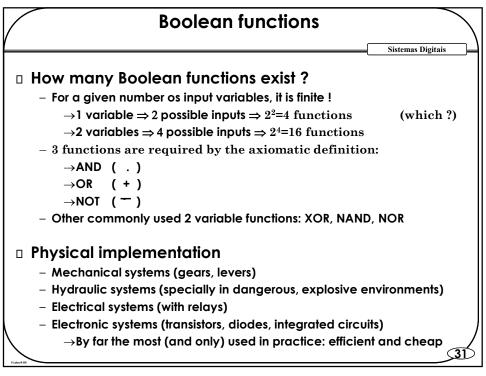
Demonstrations Sistemas Digitais Using truth tables - Show for EVERY possible case. - Truth tables for AND and OR functions S = A+B Α В S = A.B Α В

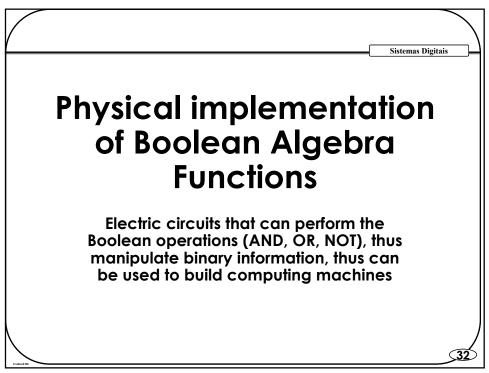
Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021

							Sistemas Digitais
0 P	rove	that /	4.(Ā	+ B) =	Α.Β		
							٦
	A	в	Ā	Ā+B	A. (Α.Β	
	0	0	1	1	0	0	
	0	1	1	1	0	0	
	1	0	0	0	0	0	
	1	1	0	1	1	1	

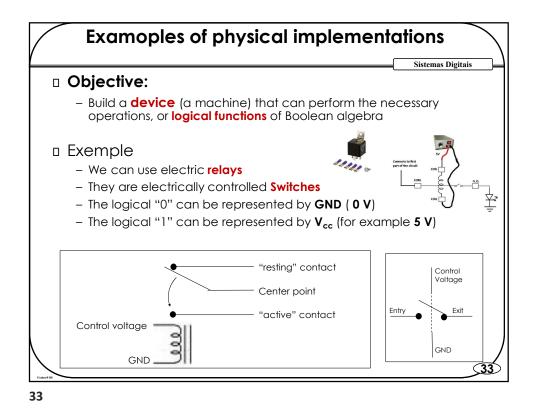


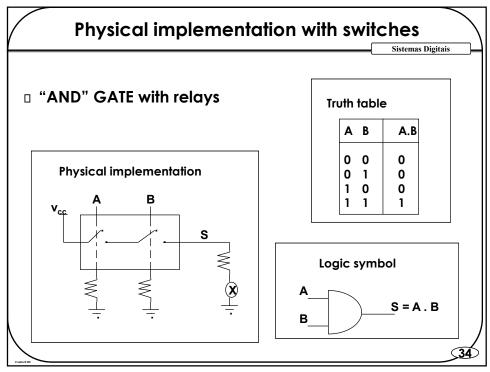
Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021

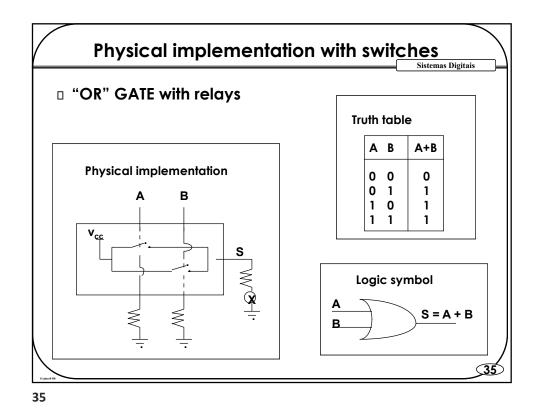


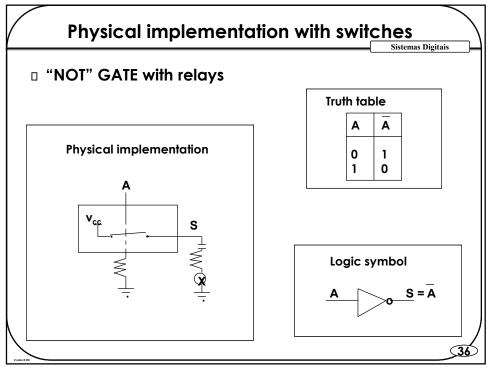


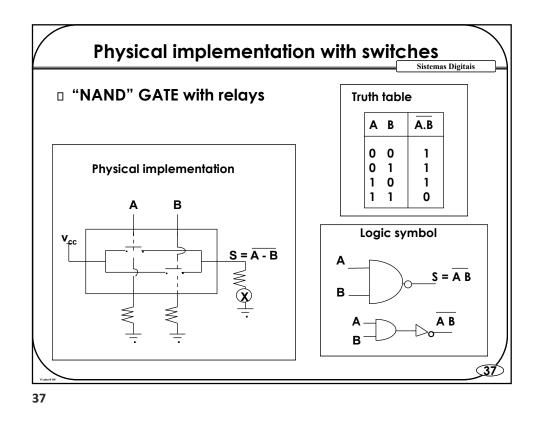
Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021

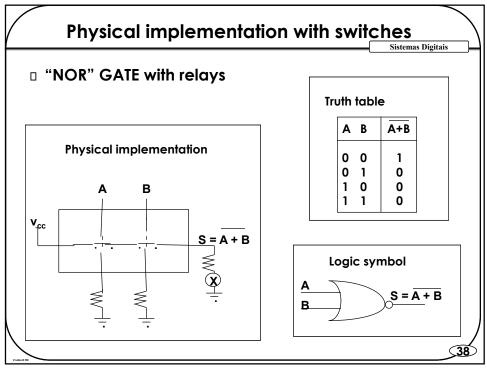


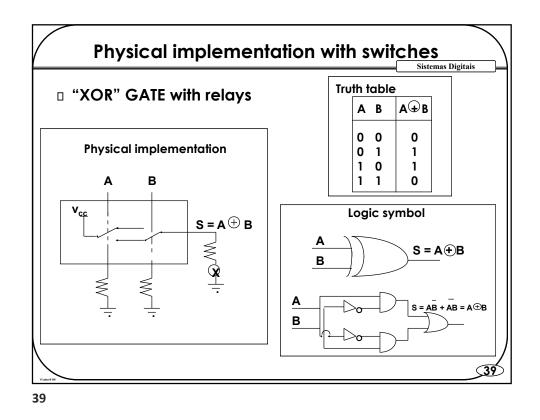


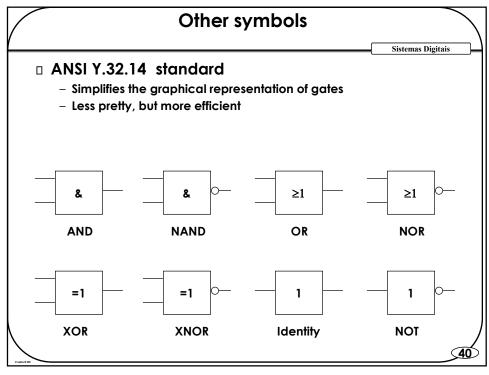


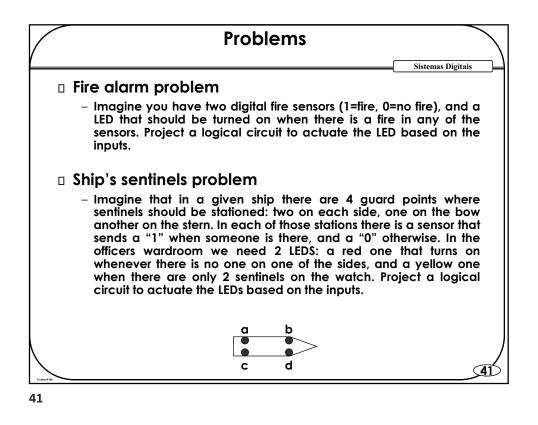


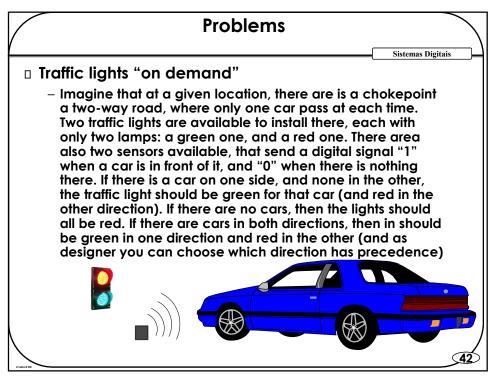


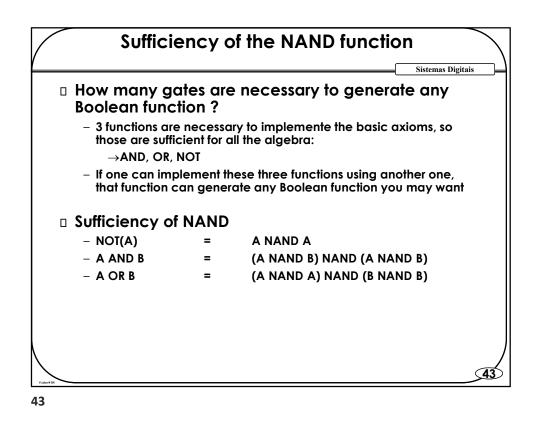


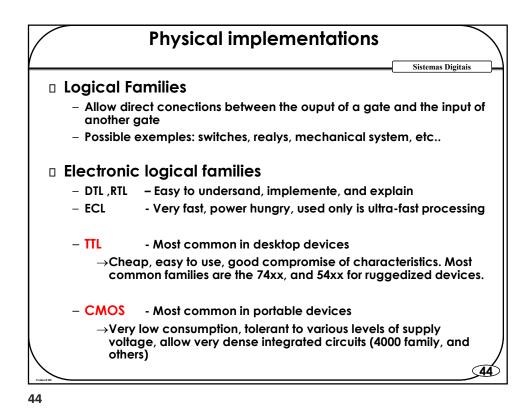




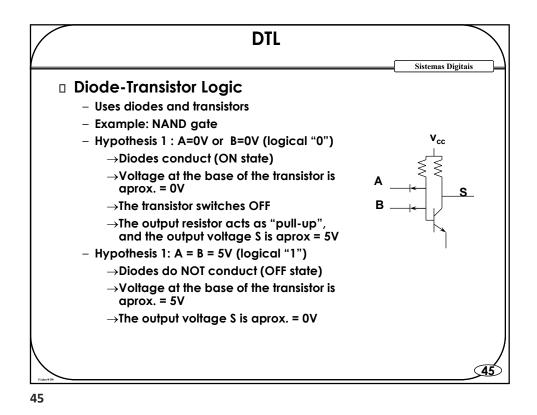


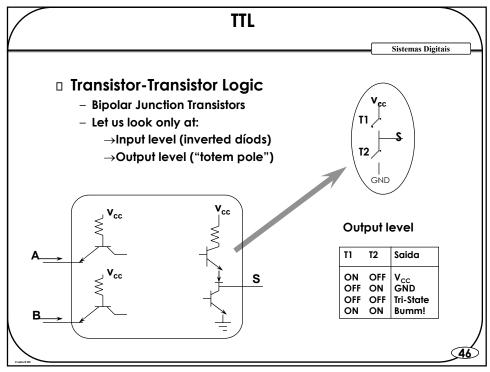


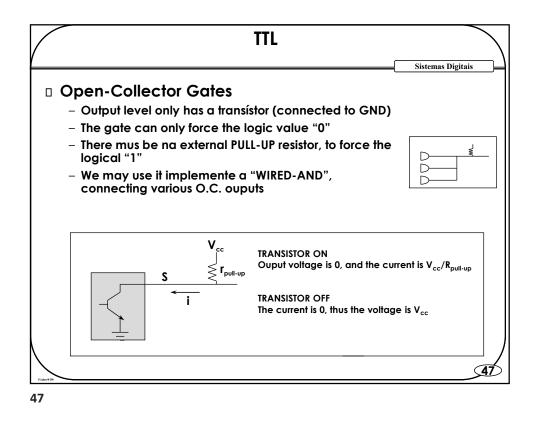


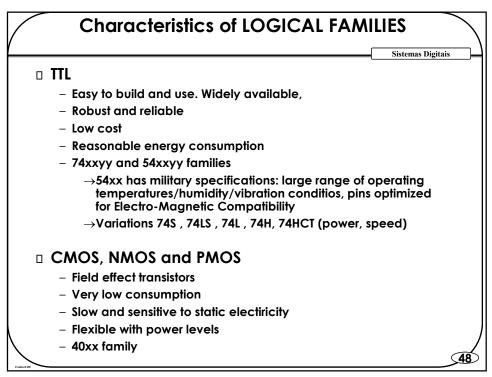


Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021

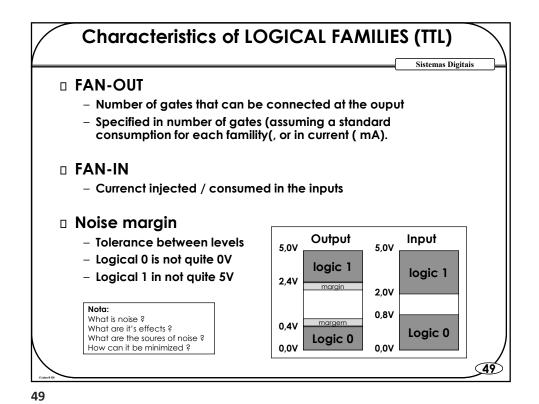






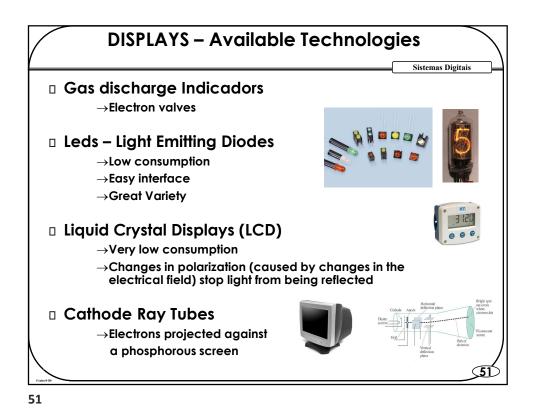


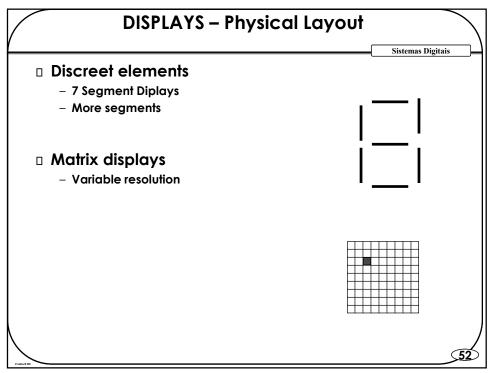
Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021

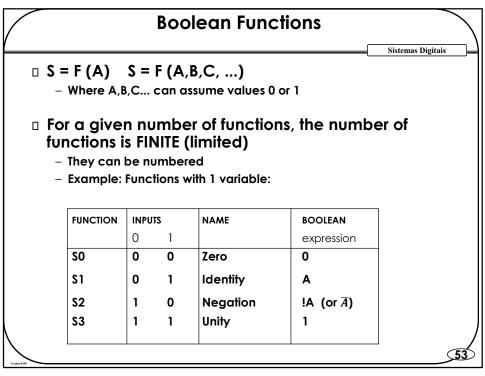


Characteristics of LOGICAL FAMILIES Sistemas Digitais GATE NOT Transfer function - Transitions $0 \rightarrow 1 \rightarrow 0$ are not perfect Gate ideal - Example: NOT gate Saída Propagation time Entrada - Gates takes a certain time until the ouptput reflects the current inputs Propagation delays when transitioning from 0 to 1 is normally different the propagation Gate real delays transitioning from 1 to 0 7ona Saído proibida **Dissipation** Entrada - Gates need current and heat up in the process - The heat produced in normally proportional to the clock frequency (50)

Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021

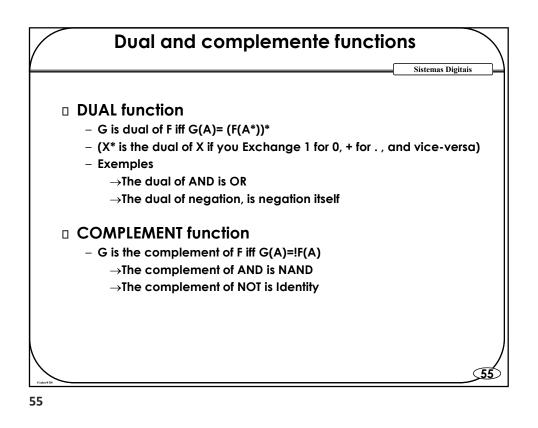


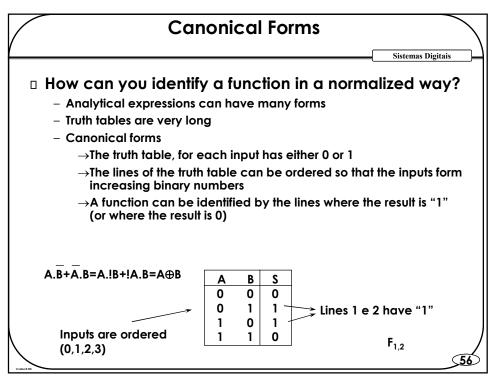




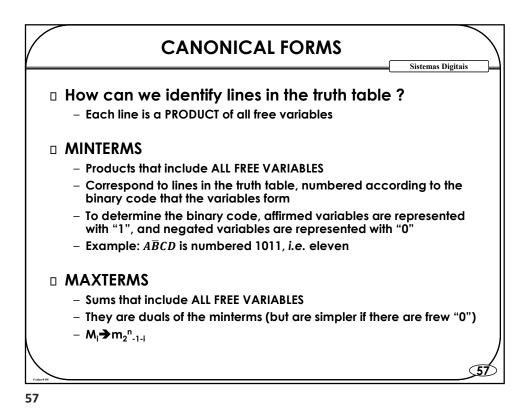
						Sistemas Di
FUNCTION	INPUTS 00 ,01,10,11	NAME	BOOLEAN Expression	NOTATION	DUAL	COMPLEMENT
SO	0000	Zero	0		15	15
S 1	0001	And	A.B	A.B	7	14
\$2	0010	Inibition or Nix	A.B*		11	13
\$3	0011	Identity (to A)	Α		3	12
S4	0100	Inibition or Nix	A*.B		13	11
\$5	0101	Identity (to B)	В		5	10
S6	0110	eXclusive OR	A*.B+A.B*	A⊕B	9	9
S7	0111	OR (Inclusive)	A+B	A+B	1	8
S8	1000	NOR (or Dagger)	(A+B)*	A+B	14	7
S9	1001	Equivalence	A.B+A*.B*	A ≡ B	6	6
S10	1010	NOT (Negation)	B*		10*	5
\$11	1011	Implication	A+B*	$B \Rightarrow A$	2	4
\$12	1100	Not (Negação)	A*		12	3
\$13	1101	Implication	A*+B	$\underline{A \Rightarrow} B$	4	2
S14	1110	NAND (or Stroke)	(A.B)*	A.B	8	1
\$15	1111	UNITY	1		0	0

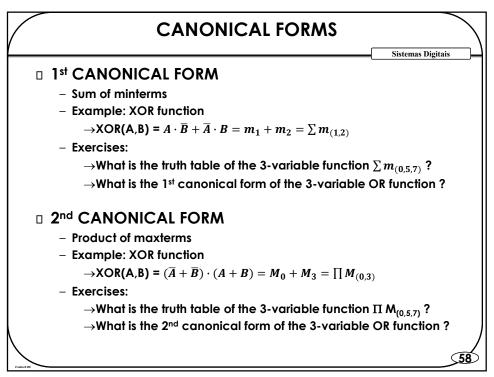
Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021



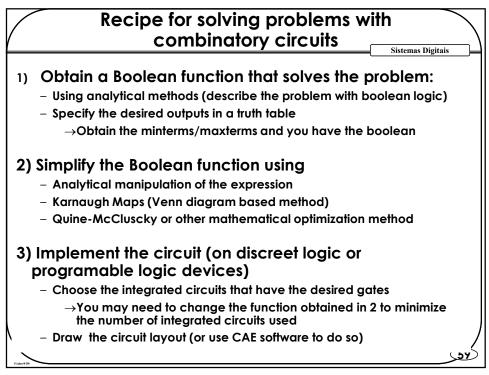


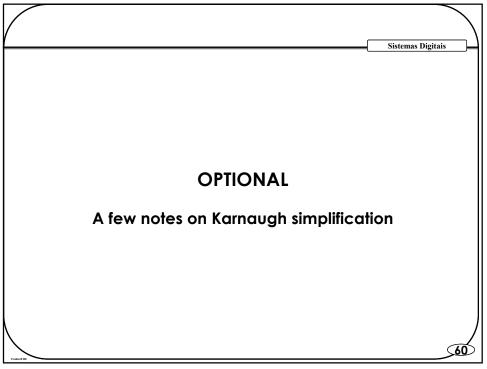
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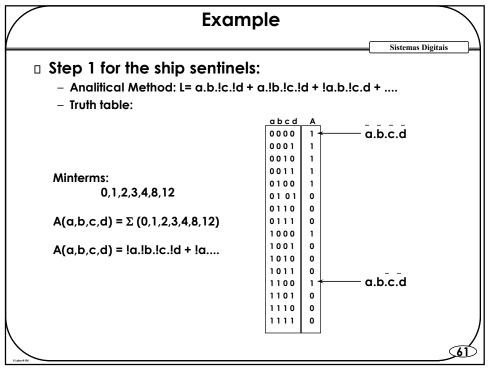


Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021

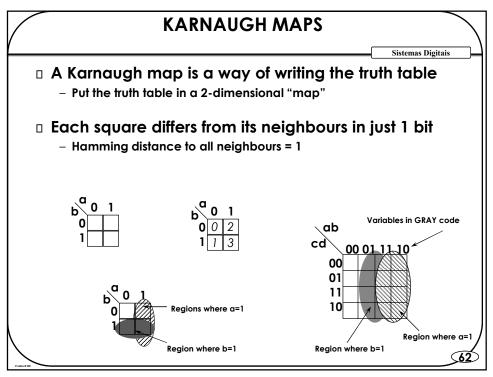


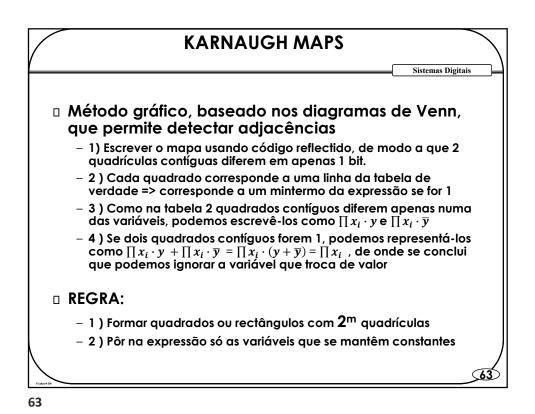


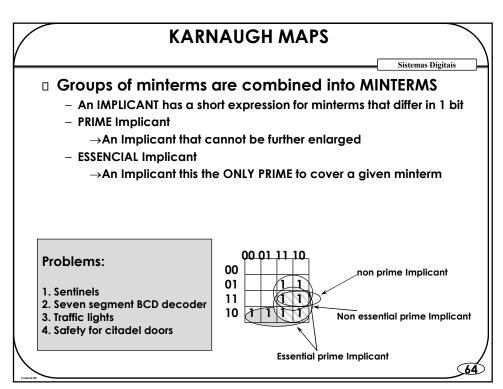
Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021



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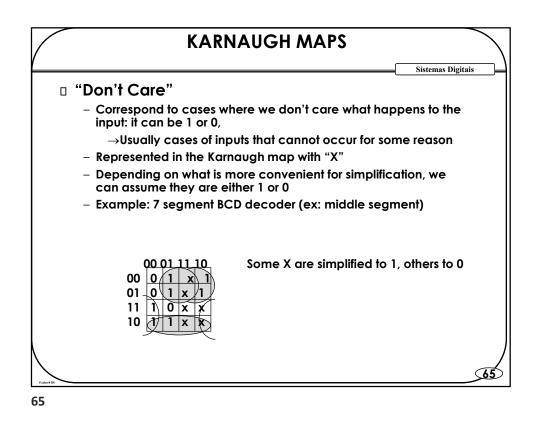


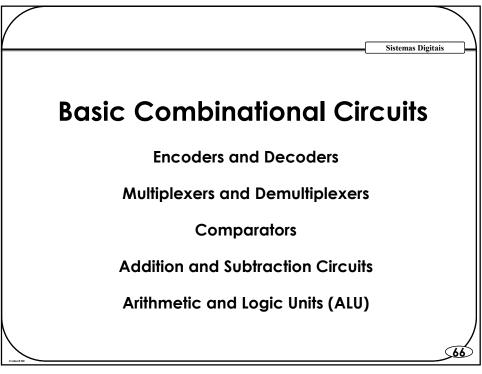




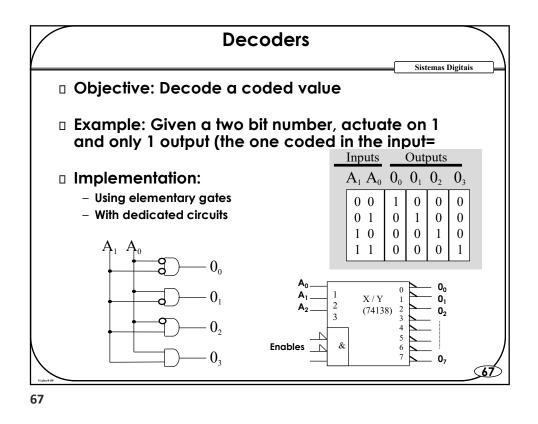


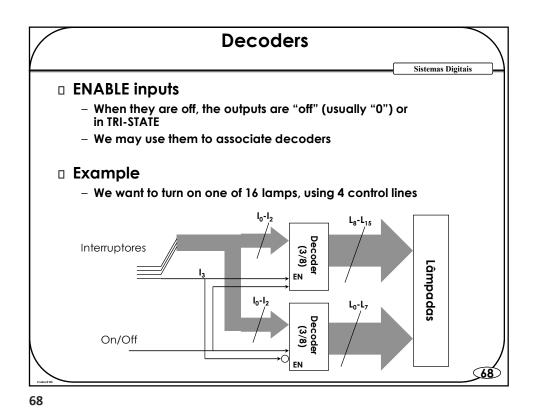
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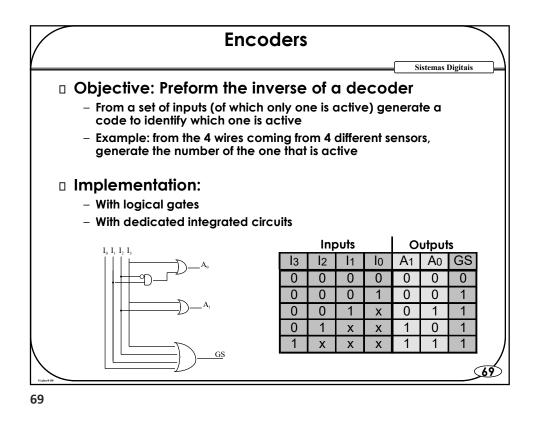
Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021

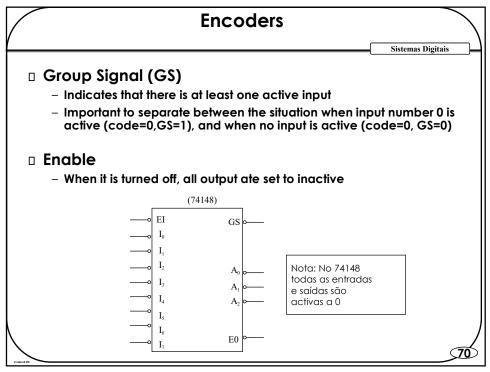


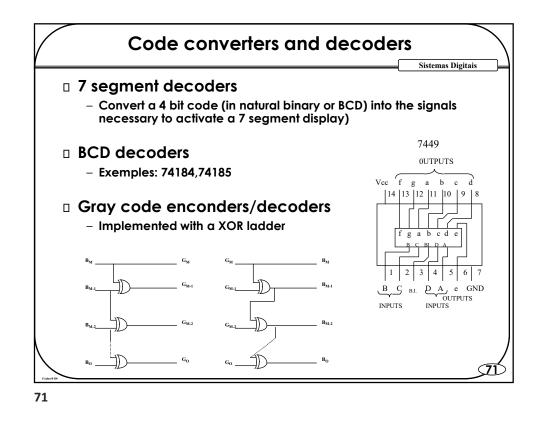


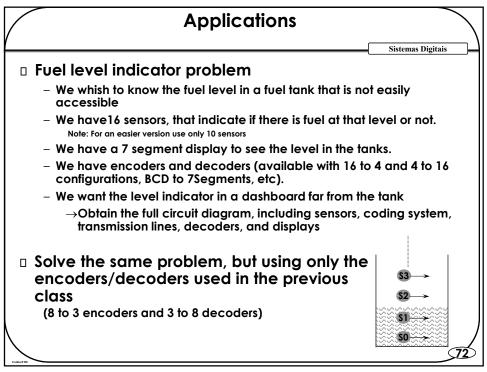
Page 34

Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021

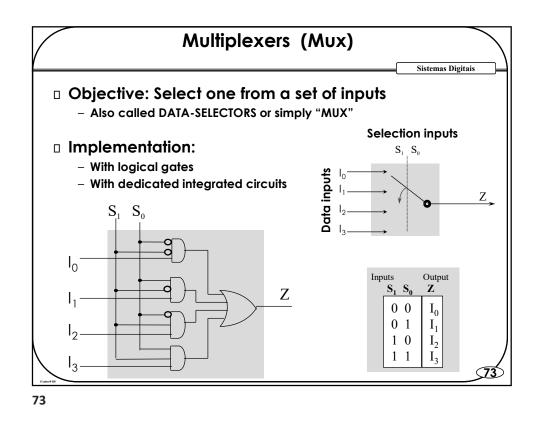


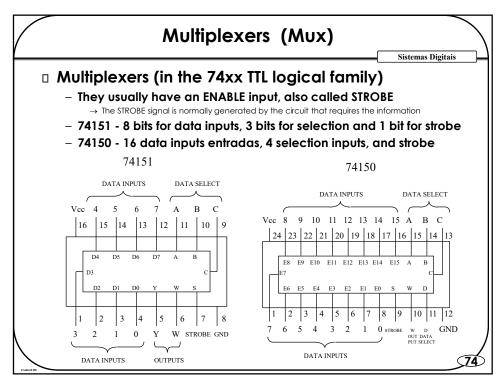




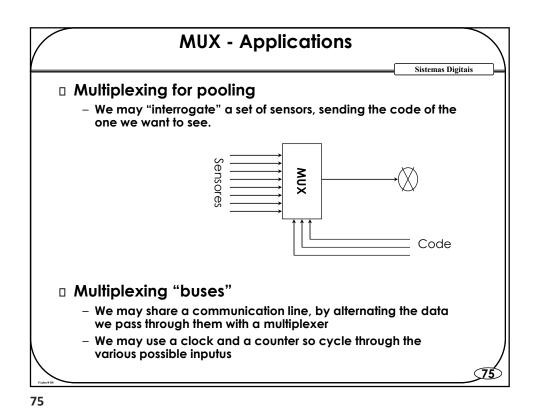


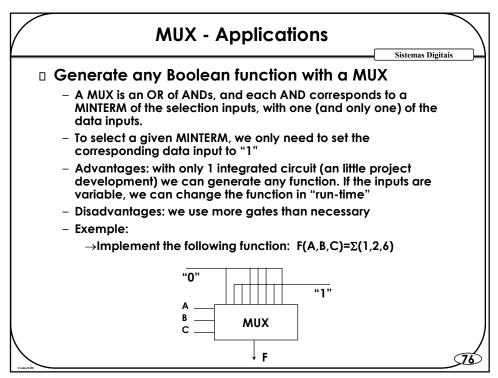
Numbering Systems, Data Representation, Boolean Algebra, Basic Ciruits V.2.4 V.Lobo 2021

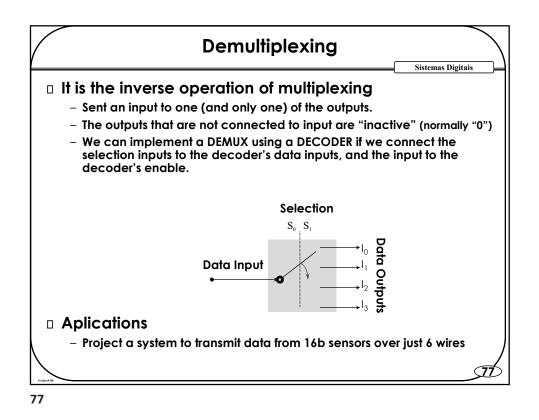


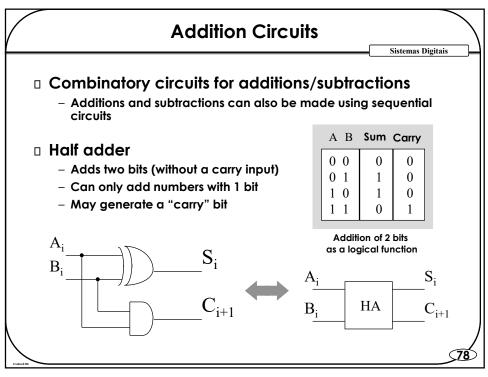


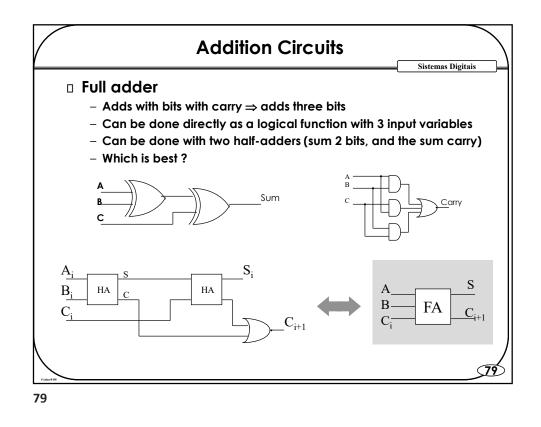
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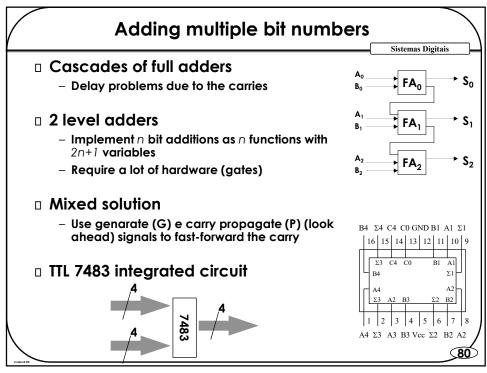




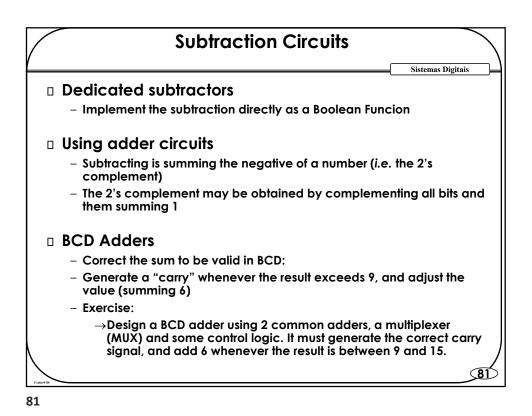








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ALU (Arithmetic and Logic Units) Sistemas Digitais Objective Perform various different arithmetic or logic operations using a single circuit, with different control signals - They normally have 2 inputs each with n bits, know as operands. - They have one (or more) control input to specify which operation is done Example: \rightarrow A ALU to perform sums and subtractions of 4 bit numbers R FA FA FA 7483 M=0 Sum M=1 Subtact C. S-S. S, (82)

