Memories

Memories

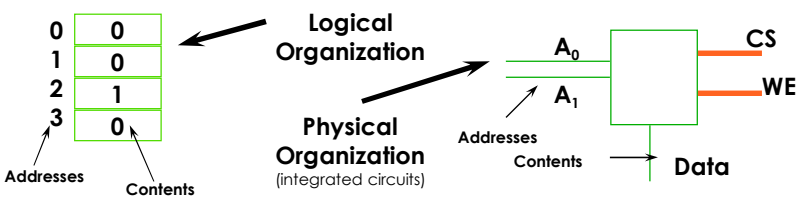
1

1

Introduction

Memories

- **Purpose of of memory system**
  - **STORE DATA** (0's and 1's)
  - **Basic Operations – WRITE a datum; READ a datum**
- **To store 1 bit only 1 flip-flop is needed**
- **To store many bits, a set of flip-flops s is necessary, and these some sort of organization.**
  - **To access a given content, one must give the ADDRESS where it is stored inside de memory, and whether we want to WRITE it or READ it.**



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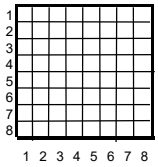
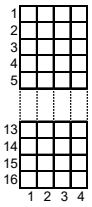
Address and memory width

Memories

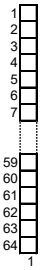
- **Data can be stored in "boxes"** (addresses) **with 1 bit, or various bits**
  - ***Width*** **of a memory is the number of bits stored in each address**
    - →**Also know as** ***word size*** **of the machine.**
  - **A "** *n* **x** *m* **" memory has** *n* **addresses, each with** *m* **bits**
  - **Most memories use 8 bits (1 byte) words.**
- **Example:** 64 bits may be organized as ...



8x8



16x4



64x1

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Types and sizes

Memories

- **The basic unit is the BIT (BI**nary digi**T)**
  - **1 Byte = 8 Bits**
  - **1 KB (Kilobyte) = 2^{10} = 1024**
  - **1 MB (Megabyte) = 2^{20} = 1.048.576**
  - **1 GB (Gigabyte) = 2^{30} = 1.073.741.824**
  - **1 TB (Terabyte) = 2^{40} = 1.099.511.627.776**
  - **1 PB (Petabyte) = 2^{50} = 1.125.899.906.842.624**

- **Many different technologies and applications**
  - **Solid state (integrated circuits)**
    - → **RAM, ROM, SRAM, DRAM, PROM, EPROM, etc**
  - **Magnetic and optical (mostly discs)**
    - →**hard drives, floppy, drums, cartridges, tapes**
    - →**Compact Disks (CD), DVD, BluRay Disks, etc**
  - **Capacities (2021)**
    - →**DRAM 1MB – 16 GB +**
    - →**SRAM,PROMs 1K – 32MB +**
    - →**HD 500GB – 20TB +**

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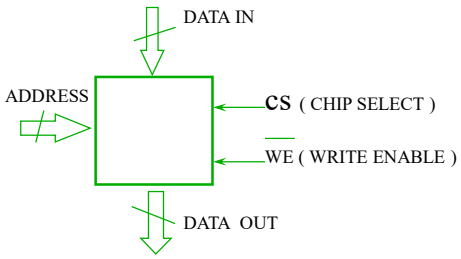
RAM Memories

Memories

- RAM- Random Access Memories (static memries)
  - You can randomly select any address (versus sequential access)
  - Built with flip-flops
  - They contain:
    - Address decoding block
    - Memory elements block
    - Control block



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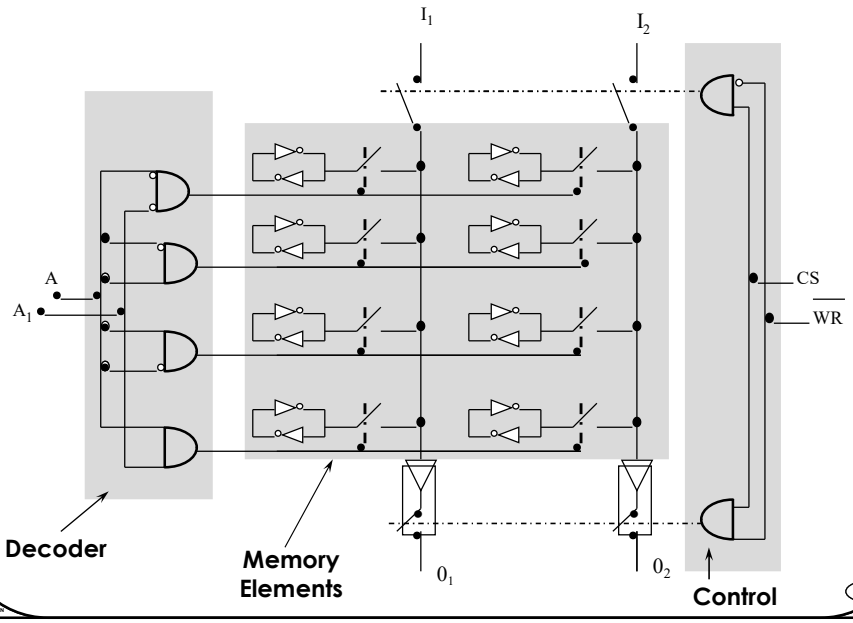
Internal organization of a RAM

Memories



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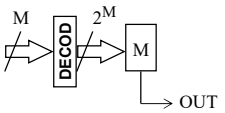
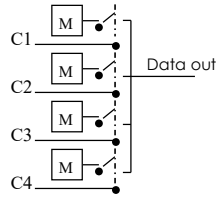
Address Decoding

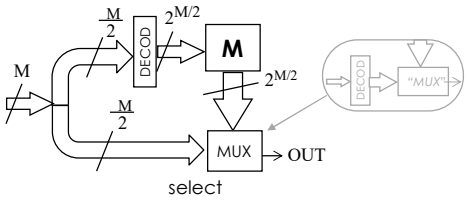
Memories

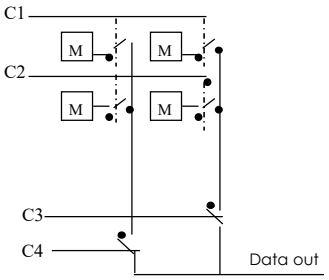
- **Linear Structure**
  - Faster, but requires more hardware





- **2 dimensional strucure**
  - Slower, less hardware





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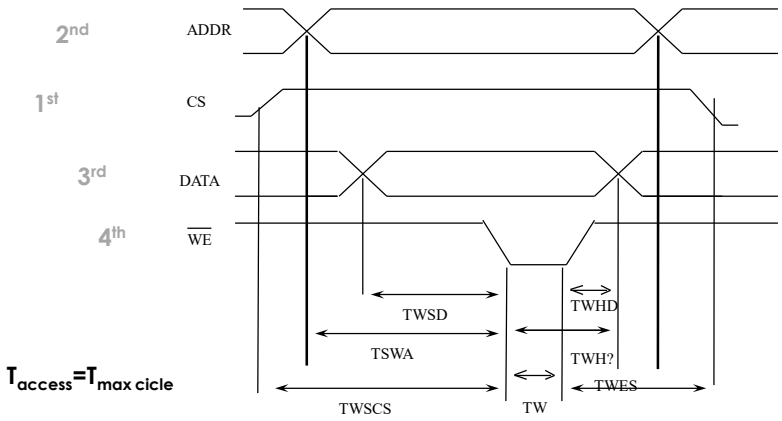
Timimg issues

Memories

- **Write cycle (a Read Cycle is similar**
  - **ADDR** - Address **CS** - Chip Select
  - **DATA** - Data to be written (or read) **WE** - Write Enable



$T_{access}=T_{max\ cicle}$

Burst mode⇒ piggyback serevel acesses to consecutive addresses

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DYNAMIC RAM MEMORIES (DRAM)

Memories

- Bits are stored in capacitors
- Advantages
  - They take much less space
  - They have much less heat dissipation
- Problems
  - They loose charge with time
  - They loose their charge when they are read
  - They need to "Refresh" their information periodically
- They need dedicated circuits to generate the "refresh cycles" periodically (2ms), that induce latency in memory access

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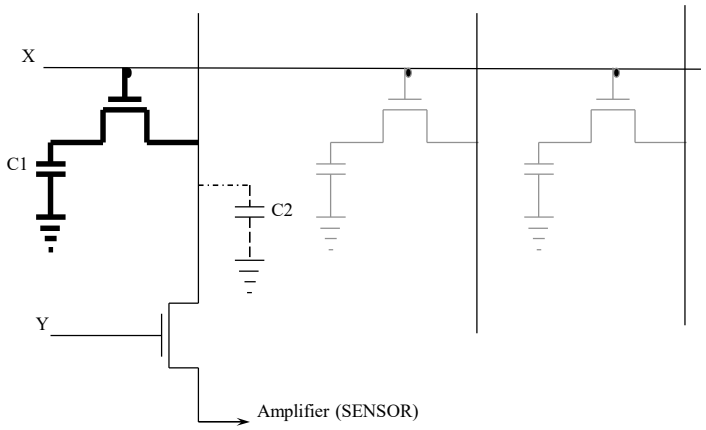
Dynamic RAM

Memories

- Basic memory block
  - 1 FET (Field Effect Transistor) + 1 Condensor (also a FET)



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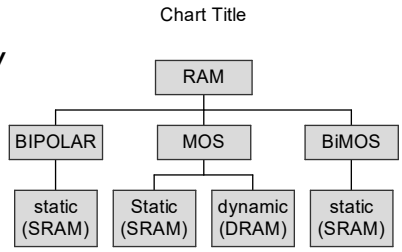
Choice of RAMS (DRAM vs SRAM)

Memories

- Factors to take into account
  - Memory size
    - →DRAMs have far mor capacity
  - Cost per bit
    - →DRAMs are cheaper
  - Physical size
    - →DRAMs are smaller
  - Power consumption
    - →DRAMs consume less energy
  - Access times
    - →SRAMs are faster, and don't have "dead time"
  - Ease of use
    - →SRAMs are easier to use (and cheaper for small capacities)



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ROM Memories

Memories

- Read Only Memory
  - Their content is pre-defined and can't be changed
  - They store "permanent" information: programs that do not change (BIOS, Firmware), tables with fixed contets (e.g. character setsin printers), etc.
- They are *not volatile*
  - Their content is not lost when power is switched off
- They are purely combinatory circuits
  - For a given input (address), they always produce the same output (datum)
  - They can be build with logical gates, using the traditional ways to implement Boolean functions
  - RAMS have no memory !!!

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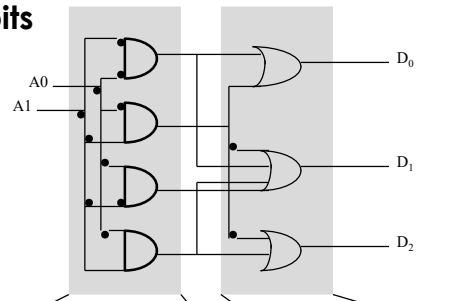
ROM Memories

Memories

- Ex: 4 addresses with 3 bits

Address	Content
00 (0)	110
01 (1)	111
10 (2)	010
11 (3)	011



Simplification with Karnaugh maps

AND plane (level)

Decodes addresses, generating all possible minterms

OR plane

Information specific to the particular content

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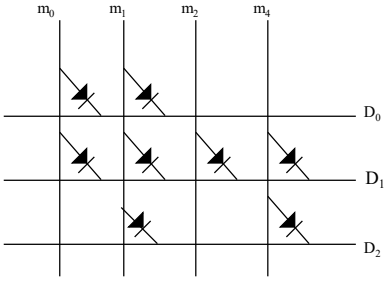
ROM Memories

Memories

- The OR plane can be substituted by a matrix of diodes
- ROMs are programed when they are built (in the factory)
  - ORs are made by inserting (or not) diodes in the junctions
  - A Mask is used (similar to those in printed circuit boards) to build them
  - Only financially viable in very large quantities



$D_0=m_0 + m_1$

$D_1=m_0 + m_1 + m_2 + m_3$

$D_2=m_1 + m_3$

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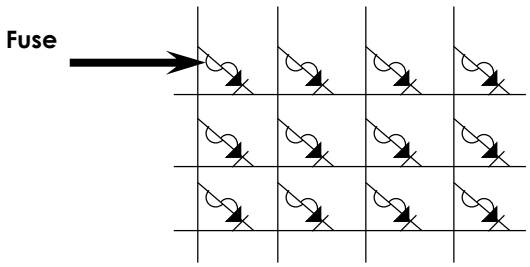
ROM Memories

Memories

- Programmable Read Only Memory
  - You can program them, but only once
  - They are similar to ROMs, but they have fuses together with diods in the line/columns junctions, that may be burned to "take out" the diode.
  - To program a PROM, the fuses are burned by storing the opposite of what we want with voltages higher than normal (PROMs are "blown out")



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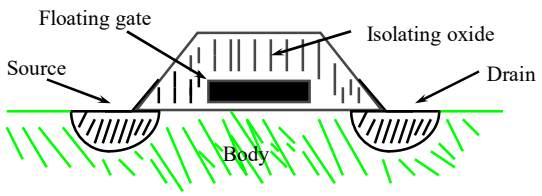
EPROM Memories

Memories

- Erasable Programable Read Only Memory
  - It is possible to erase the content, and re-program it
  - The erasure/reprograming takes time
  - FAMOS (Floating-Gate Avalanche-Injection Metal Oxide Semiconductor) devices are used.
    - →They are MOS-FETs with an isolated (floating) gate
    - →The charge stores in the gate puts the FET in conducting or isolating mode
    - →The floating gate can be electrically charged using high negative voltage and tunneling effect.
    - →The floating gate can be discharged using ultraviolet radiation that makes the oxide a conductor.



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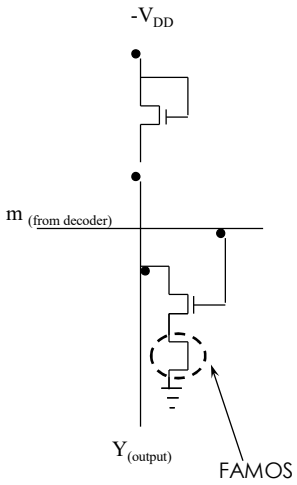
EPROM Memories

Memories

- Erasing can take about 10 minutes under a UV lamp
  - It is not practical to reprogram when in use
  - The integrate circuits have a class window to allow the light in
- It may programed BYTE by BYTE
  - A FAMOS will be discharged (and the logical content will be "1") until voltage is applied to charge it
  - We may program it one address at a time (converting the 1s to 0s)



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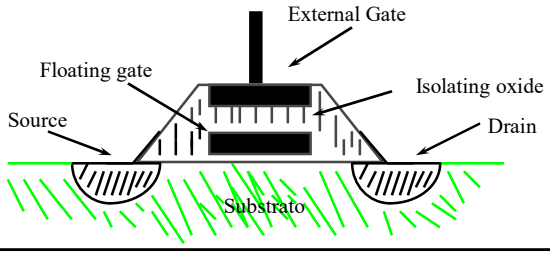
E²PROM or EEPROM Memories

Memories

- Electrically Erasable Prom
  - Use STACKED GATE FET
    - →FETs with a floating gate between the base and the external gate
    - →The channel under gate is turned ON/OFF by the floating gate, that is charged and discharged by the external gate by tunneling/avalanche
    - →They take aprox. 1s to program
    - →They used to be very expensive and not used much until "flash" technology made them cheap and popular, and are known as "flash memories"



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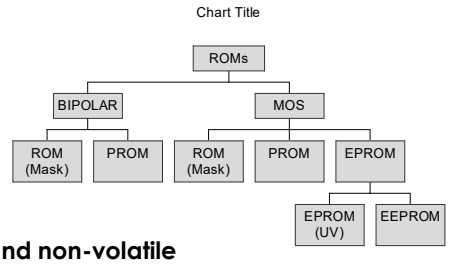
Choice of ROM Memories

Memories

- **Factors to take into account choosing ROMS**
  - **Quantity**
    - **→PROMs are cheaper (they are always built in quantity)**
  - **Stability of information**
    - **→EPROMs better during the design phase (they may be corrected)**
  - **Need to reprogram frequently**
    - **→EEPROM are more versatile, but EPROM may be acceptable**



- **Applications**
  - **Startup code**
  - **Code that doesn't change**
  - **Code that has to be robust and non-volatile**
  - **Code converters (bin/bcd, bcd/7 seg, etc)**
  - **Control (sensors/alarms/actuators)**

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Memories

Other technologies used in memories

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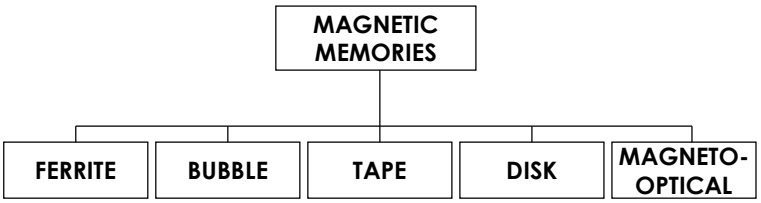
Magnetic memories

Memories

- Used mainly as secondary memories
- Sequential access
  - Tapes ("normal" tapes, cartridges , DAT, etc), Disks (hard drives and floppy)
- Random access
  - Ferrite, Magnetic bubble (that has latency times)



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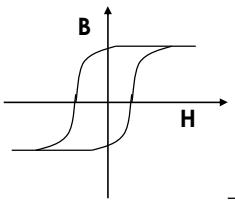
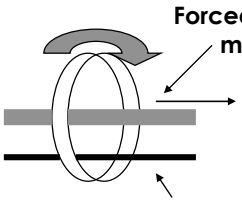
FERRITE MEMORIES

Memories

- Basic principle
  - A ferrite torus can be magnetized in two different directions (one for each logic value)
  - To magnetize it, simply pass a high current through its center
  - To "measure" the magnetization, we need to measure the impedance it offers to a low current

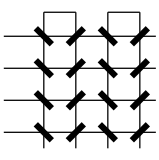


Hysteresis loop



Forced current induces magnetization

Sensor wire where the impedance is measured



Torus matrix

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MAGNETIC MEMORIES

Memories

- **Ferrite memory's features**
  - Very low density (torus are macroscopic!)
  - Long access time
  - Destructive reading
  - Non-volatile memory
- **Magnetic bubble memories**
  - Weiss' domains are individually manipulated
  - Large latency times
  - High density

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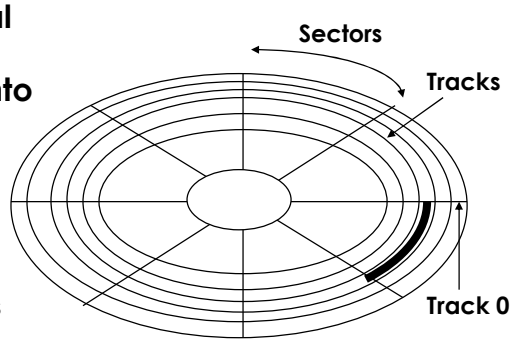
DISKS

Memories

- **Keeps information about one (or multiple) surfaces of magnetic material**
- **The disk is divided into**
  - Sectors
  - Tracks (or cylinders)
  - Heads (or surfaces)
- **Formatting**
  - Creation of the markers
  - Track numbering



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FLOPPY DISKS & MAGNETIC TAPES

Memories

- **Floppy disks**
  - Are flexible
  - Heads "scrape" the surface
  - Cheap, but slower and less dense hard disks
  - Sizes: 8", 5¼", 3½" (most common, with 1440KB), 3" .

- **Magnetic Tapes**
  - Very similar to audio magnetic tapes
  - Have MARKERS to perform quick searches, followed by data REGISTERS
  - Used as backup, or to download massive amounts of data

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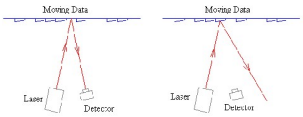
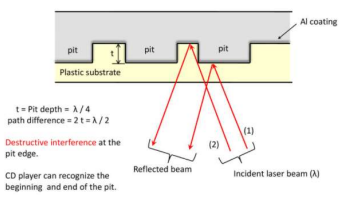
Optical Compact Disks

Memories

- **Various Formats**
  - Most common is the 120mm CD (Sony&Philips, 1982)
    - →Up to 700Mb, 74 min HiFi (44kHz,16 bit, 2 channels)
    - →"upgrades" to CD-W, CD-R, CD-RW, DVD…
  - VideoCD, SVDC, PCD, MiniCD,…

- **Main characteristics**
  - Information is coded in "Pits" with different lengths (0 and 1)
  - Light is reflected of an uneven surface
  - Constant linear density ⇒variable angular velocity (spiral)
  - Different capacities (up to 17GB) depend on:
    - →Type of laser used
    - →Number of surfaces
    - →"Mask" CD, CD-Rom, & CD-RW





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Other memory system organizations

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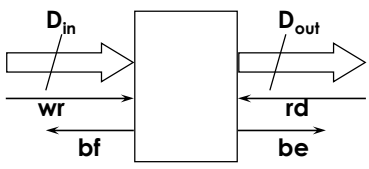
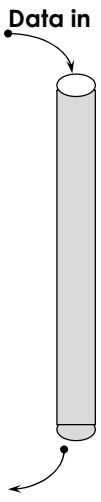
FIFO or ELASTIC MEMORIES

- First In First Out
- Structure similar to a Shift Register:
  - The data goes in by one side and out by the other
  - Unlike Shift Register it can be partially full
  - Similar to a tube where the data is placed on one side and removed from the opposite side
- How it works
  - Has signals which indicate if they're full/empty
  - To write: verify the Buffer Full signal and then activate Write
  - To read: verify the Buffer Empty signal and then activate Read





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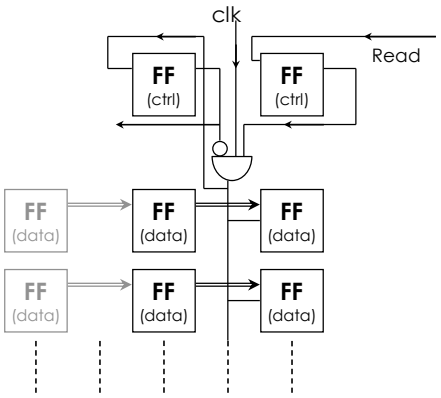
FIFO or ELASTIC MEMORIES

Memories

- **Implementation**
  - It is necessary to manage occupied and free positions
  - There's a set of auxiliary flip-flops which indicate if a position is free or not (1 = free, 0 = occupied)
  - There's other types of implementations (shift regs w/ reading control)



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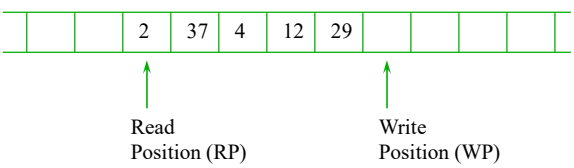
FIFO or ELASTIC MEMORIES

Memories

- **Applications**
  - →Buffer to adapt 2 systems of different speeds
  - →Communications; Buffer queues; Control, etc.
- **Can be simulated with conventional memory**
  - 2 pointers are used: one for reading, another for writing
  - To write:
    - →Verify BP; Write in WP position and increment WP ; If WP=MAX ⇒ WP=0; if WP=RP ⇒ BF
  - To read:
    - →Verify BE; Read in RP position ; If RP=MAX ⇒ RP=0; if RP=WP ⇒ BE



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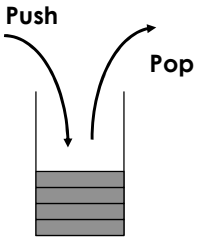
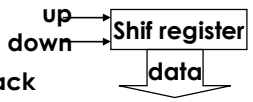
LIFO MEMORIES

Memories

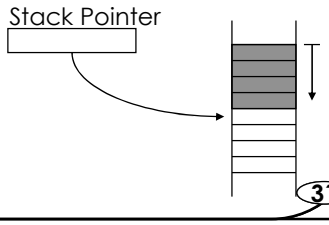
- **LIFO - Last in, first out**
  - Also called STACKs
  - The last one in is the first one out
  - "Push-down stack"



- **Operation**
  - PUSH - Put data in the Stack
  - POP - remove data from the Stack



- **Implementation**
  - With a bidirectional shift-register
  - In software
    - →Stack Pointer
    - →Memory reserved zone
    - →PUSH and POP routines



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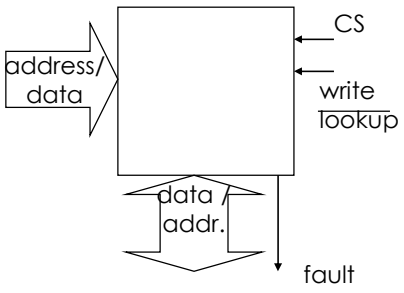
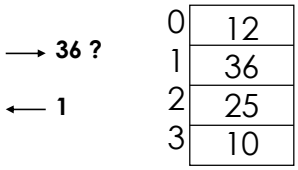
ASSOCIATIVE MEMORIES

Memories

- **Also called *addressable* by content**
- **Given a content, an address is obtained**
  - Relates a content to an address
  - "addresses" with the content
- **Applications**
  - Indexes
  - Virtual memory systems





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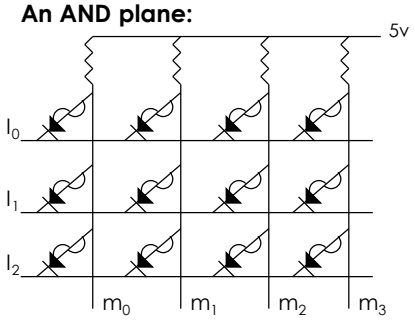
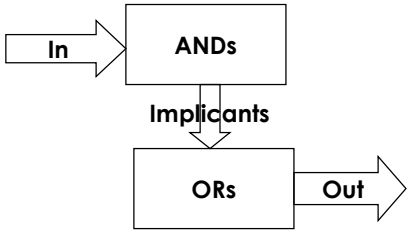
PLD - Programmable Logic Devices

Memories

- **Similar to PROMs**
  - Has an AND plane followed by an OR plane
  - They are used to generate Logic Functions
  - Unlike ROMs, do NOT have all the MINTERMS
  - Although very flexible and versatile, due to the lack of some degrees of freedom, they can't generate any function

An AND plane:





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PLD - Programmable Logic Devices

Memories

- **PLA - Programmable Logic Array**
  - Both planes (ORs and ANDs) are programmable
- **PAL - Programmable Array Logic**
  - Only the ANDs plane is programmable
- **Others**
  - PLS (Programmable logic sequencer)
  - FPA (Field Programmable Array)
  - FPGA (Field Programable Gate Array), etc.
- **Advantages**
  - Much cheaper and easier to assemble than discrete logic
  - Much cheaper than ASIC (Application Specific Integrated Circuits)
  - More efficient and cheaper than full PROMs
  - Easily programmable with software assistance
  - May implement more complex functionalities (full microprocessor)

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MEMORY BANKS

Memories

- **Concept of ADDRESS SPACE**
  - Addresses that can be generated with a given number of bits
  - May or may not correspond to physical memory
  - Ex: 8085 has 16 bits address, therefore an address space of 64K; the Pentium II has 32 bits of addresses, therefore an address space of 4G
- **Memory insertion in an address space**
  - The physical memory is MAPPED to addresses from the machine's address space
  - Some bits from the address are used to generate the Chip Select (CS)
    - →The address to where the physical memory is mapped depends on the function used to generate the CS
    - →Some address bits are used to access the several positions inside the memory

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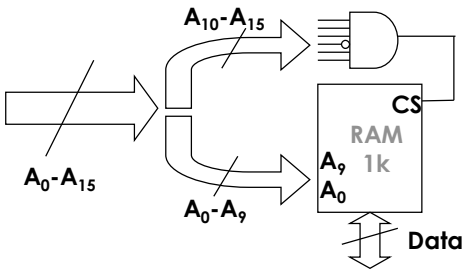
MEMORY BANKS

Memories

- **Example:**
  - Insert a 1K physical memory in a address space generated by 16 address bits, in order to map it for the addresses between 4 and 5K.
  - Solution
    - →A 1K memory needs $\log_s(1k)=10$ bits for internal addressing
    - →The remaining 6 address bits will be used to generate the CS
    - →When those 6 bits form the number 4, the CS should be 1



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MEMORY BANKS

Memories

- **Interlaced memories**
  - It isn't necessary for the most significant bits to be used to generate the CS
  - What happens if we use the least significant?
- **Memory replication**
  - It isn't necessary to completely decode the addresses
  - What happens if we don't use all the "leftover" bits for the CS?

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MEMORY BANKS

Memories

- **Problem**
  - A data system based on a microprocessor has a 16 bit address bus and a 8 bits data bus.
  - The goal is to have ROM memory in the first 8K addresses, and RAM memory from addresses 8000H to A000H.
  - You have at your disposal 8K×4 bits ROM memory integrated circuits, and 1K×8 bits RAM memory integrated circuits.
  - Draw the intended memory system's scheme.

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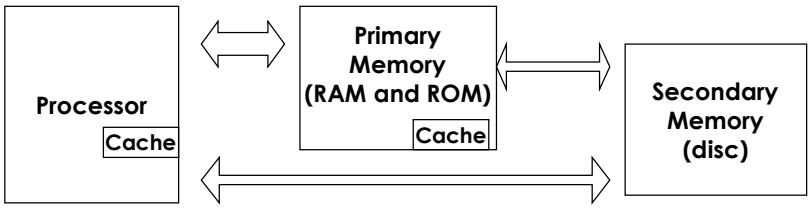
MEMORY HIERARCHY

Memories

- Cache memory
- Main or Primary memory
- "Mass" or Secondary memory



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