

JUMP

C3 JMP
 C2 JNZ
 CA JZ
 D2 JNC
 DA JC
 E2 JPO
 EA JPE
 F2 JP
 FA JM
 E9 PCHL

CALL

CD CALL
 C4 CNZ
 CC CZ
 D4 CNC
 DC CC
 E4 CPO
 EC CPE
 F4 CP
 FC CM

RETURN

C9 RET
 C0 RNZ
 C8 RZ
 D0 RNC
 D8 RC
 E0 RPO
 E8 RPE
 F0 RP
 F8 RM

RESTART

C7 RST 0
 CF RST 1
 D7 RST 2
 DF RST 3
 E7 RST 4
 EF RST 5
 F7 RST 6
 FF RST 7

ROTATE†

07 RLC
 0F RRC
 17 RAL
 1F RAR
 CONTROL

MOVE (cont)

58 MOV E,B
 59 MOV E,C
 5A MOV E,D
 5B MOV E,E
 5C MOV E,H
 5D MOV E,L
 5E MOV E,M
 5F MOV E,A

60 MOV H,B
 61 MOV H,C
 62 MOV H,D
 63 MOV H,E
 64 MOV H,H
 65 MOV H,L
 66 MOV H,M
 67 MOV H,A

ACCUMULATOR*

80 ADD B
 81 ADD C
 82 ADD D
 83 ADD E
 84 ADD H
 85 ADD L
 86 ADD M
 87 ADD A

88 ADC B
 89 ADC C
 8A ADC D
 8B ADC E
 8C ADC H
 8D ADC L
 8E ADC M
 8F ADC A

CONSTANT-DEFINITION

0BDH } Hex
 1AH }

105D } Decimal
 105 }

720 } Octal
 72Q }

11011B } Binary
 00110B }

'TEST' } ASCII
 'A' 'B' }

MOVE IMMEDIATE

06 MVI B,
 0E MVI C,
 16 MVI D,
 1E MVI E,
 26 MVI H,
 2E MVI L,
 36 MVI M,
 3E MVI A,

LOAD IMMEDIATE

01 LXI B,
 11 LXI D,
 21 LXI H,
 31 LXI SP,

DOUBLE ADD†

09 DAD B
 19 DAD D
 29 DAD H
 39 DAD SP

STACK OPS

C5 PUSH B
 D5 PUSH D
 E5 PUSH H
 F5 PUSH PSW

C1 POP B
 D1 POP D
 E1 POP H
 F1 POP PSW*

**20 RIM
 30 SIM**

SPECIALS

EB XCHG
 27 DAA*
 2F CMA
 37 STC†
 3F CMCT

INPUT/OUTPUT

D3 OUT } D8
 DB IN }

OPERATORS

(.)
 *./, MOD, SHL, SHR
 +,
 NOT
 AND
 OR, XOR

INCREMENT**

04 INR B
 0C INR C
 14 INR D
 1C INR E
 24 INR H
 2C INR L
 34 INR M
 3C INR A

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INCREMENT**

04 INR B
 0C INR C
 14 INR D
 1C INR E
 24 INR H
 2C INR L
 34 INR M
 3C INR A

DECREMENT**

05 DCR B
 0D DCR C
 15 DCR D
 1D DCR E
 25 DCR H
 2D DCR L
 35 DCR M
 3D DCR A

LOAD/STORE

0A LDAX B
 1A LDAX D
 2A LHLD Adr
 3A LDA Adr

SPECIALS

EB XCHG
 27 DAA*
 2F CMA
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 3F CMCT

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STACK FORMAT

7 6 5 4 3 2 1 0

S | Z | 0 | 1 | 2 | P | 1 | C

MACRO ()

ADR = 16 bit address

** = all Flags except CARRY affected;
 (exception: INX & DCX affect no Flags)

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